

## CLAIMS

1. A method for control of a converter for conversion of dc voltage into ac voltage or dc voltage and vice versa, comprising a series connection of four units (S1-S4), arranged between two poles, one positive pole (7) and one negative pole (8), of a first side in the form of a dc-voltage side of the converter, each of said units comprising a gate turn-off semiconductor element (13-16) and a diode (17-20) connected in antiparallel therewith and being given orders according to the order in the series connection from the positive to the negative pole, a line on the second side of the converter being connected to a first centre, designated output (4), of the series connection between the second and third units, means (9) arranged to provide, on said first side, a centre (23) between the two poles and to place these poles at the same voltage but with opposite signs in relation to the centre of the first side, wherein a second centre (24) of the series connection between the first and second units is connected, via a fifth said unit (S5) with a gate turn-off semiconductor element (10) and with the diode (26) connected in antiparallel therewith with the conducting direction with respect to the output (4) opposite to the conducting direction of the diode of the second unit, to the centre (23) of the first side, and a third centre (27) of the series connection between the third and fourth units is connected, via a sixth said unit (S6) with a gate turn-off semiconductor element (11) and with the diode (29) connected in antiparallel therewith with a conducting direction with respect to the output opposite to the diode of the third unit, to the centre of the first side, wherein the semiconductor elements of the units are controlled to be turned on and off such that alternately four main states are obtained in the converter in the form of a connection of the output (4) to the positive pole (7) of the first side according to a first, to the negative pole (8) according to a second, or the centre (23) via any of two different so-called zero states, namely, a third, in which the second and fifth units are in a conducting state, and a fourth, in which the third

and sixth units are in a conducting state, wherein the first and sixth units form a pair in that said semiconductor elements are controlled to assume, in the respective main state, the same position, turned on or off, and the fourth and fifth units form a pair in that these semiconductor elements are controlled to assume, in the respective main state, the same position, turned on or off, and wherein a change between the first and second main states is always made via the third or fourth zero state, **characterized** in that, when changing between main states via a so-called small commutation loop, that is, changing between a connection of the positive pole (7) to the output (4) and the zero state according to the third main state, or changing between a connection of the negative pole (8) to the output (4) and the zero state according to the fourth main state, at least when the current direction would entail a voltage peak on essentially the entire voltage between said positive pole and said negative pole across that of the second or the third unit (S2, S3) which does not belong to the commutation loop in those cases where the semiconductor elements which are to be turned on in the coming main state and belong to a said pair (S1, S6 and S4, S5, respectively) of units were to be turned on simultaneously, an extra sequence is carried out in the form of a delayed turn-on of the semiconductor element in one unit of the latter pair relative to the semiconductor element in the other unit of said pair.

2. A method according to claim 1, **characterized** in that said extra sequence is always carried out when changing main states according to a said small commutation loop independently of the current direction at the output.

3. A method according to claim 1 or 2, **characterized** in that it is the semiconductor element in the outer unit (S1, S4), that is, the first or fourth unit, of the respective pair of units that is turned on with a delay relative to the other unit (S6, S5), that is, the sixth or fifth, in the pair.

4. A method according to any of the preceding claims,  
characterized in that, when changing from the first to the  
third main state, the semiconductor element in the fourth  
unit (S4) is turned on with a delay relative to the semi-  
5 conductor element in the fifth unit (S5).
5. A method according to any of the preceding claims,  
characterized in that, when changing from the second to the  
fourth main state, the semiconductor element in the first  
10 unit (S1) is turned on with a delay relative to the semi-  
conductor element in the sixth unit (S6).
6. A method according to any of the preceding claims,  
characterized in that, when changing from the third to the  
15 first main state, the semiconductor element in the first  
unit (S1) is turned on with a delay relative to the semi-  
conductor element in the sixth unit (S6).
7. A method according to any of the preceding claims,  
20 characterized in that, when changing from the fourth to the  
second main state, the semiconductor element in the fourth  
unit (S4) is turned on with a delay relative to the semi-  
conductor element in the fifth unit (S5).
- 25 8. A method according to any of the preceding claims,  
characterized in that said delay is smaller than one tenth,  
preferably smaller than one-hundredth, of the normal dura-  
tion of a said main state.
- 30 9. A method according to any of the preceding claims,  
characterized in that the semiconductor elements of the  
units are controlled such that, between two main states, a  
so-called blanking state (B) is always achieved to avoid  
that semiconductor elements that are not allowed to be  
35 turned on simultaneously should briefly be so, at least  
partly, and that, during this state, such a semiconductor  
element has time to turn off before another such element is  
thereafter turned on.

10. A method according to claim 9, **characterized** in that the semiconductor elements are controlled to assume said blanking state (B) for a period of time that lasts less than one-tenth, preferably less than one-hundredth, of the normal  
5 duration of a said main state.

11. A method according to any of the preceding claims, **characterized** in that the first main state is achieved by controlling the semiconductor elements in the first (S1),  
10 second (S2) and sixth (S6) units to be turned on, the second main state by controlling the semiconductor elements in the third (S3), fourth (S4) and fifth (S5) units to be turned on, the third main state by controlling the semiconductor elements in the second (S2), fourth (S4) and fifth (S5)  
15 units to be turned on, and the fourth main state by controlling the semiconductor elements in the first (S1), third (S3) and sixth (S6) units to be turned on.

12. A method according to claim 11, **characterized** in that,  
20 when changing from the first main state to the third main state, the semiconductor elements in the first (S1) and sixth (S6) states are first turned off, then the semiconductor element in the fifth (S5) unit is turned on, and finally the semiconductor element in the fourth unit (S4) is  
25 turned on.

13. A method according to claim 11, **characterized** in that, when changing from the third main state to the first main state, the semiconductor element in the fourth unit (S4) is  
30 first turned off, then the semiconductor element in the sixth unit (S6) unit is turned on, whereupon the semiconductor element in the fifth unit (S5) is turned off, and, finally, the semiconductor element in the first unit (S1) is turned on.

35 14. A method according to claim 11, **characterized** in that, when changing from the second main state to the fourth main state, the semiconductor elements in the fourth (S4) and fifth (S5) units are first turned off, then the semiconductor

element in the sixth unit (S6) unit is turned on, and, finally, the semiconductor element in the first unit (S1) is turned on.

5 15. A method according to claim 11, characterized in that, when changing from the fourth main state to the second main state, the semiconductor element in the first unit (S1) is first turned off, then the semiconductor element in the fifth  
10 unit (S5) unit is turned on, whereupon the semiconductor element in the sixth unit (S6) is turned off, and, finally, the semiconductor element in the fourth unit (S4) is turned on.

16. A method according to any of the preceding claims,  
15 characterized in that the semiconductor elements are controlled to minimize the duration of states, lying between said main states, with the semiconductor elements in the second (S2) and sixth (S6) units being simultaneously turned on, or those in the third (S3) and fifth (S5) units being  
20 simultaneously turned on to avoid parallel currents in the converter.

17. A method according to any of the preceding claims, characterized in that, when changing between main states via  
25 a large commutation loop, that is, when changing between the first main state and the fourth main state or when changing between the second main state and the third main state, the semiconductor elements belonging to the same pair of units (S1, S6 and S4, S5, respectively) are controlled with one  
30 and the same control pulse to be both maintained constantly in the same position, turned off or on, during the changing.

18. A method according to any of the preceding claims, characterized in that the semiconductor elements of the  
35 units are controlled such that the two zero states are assumed essentially the same number of times per unit of time.

19. A method according to claim 18, **characterized** in that the semiconductor elements of the units are controlled such that essentially each time a said zero state is to be chosen, that zero state is chosen which is opposite to the zero state which, with respect to time, immediately precedes it.

20. A method according to any of the preceding claims, **characterized** in that it is carried out on a converter with several said semiconductor elements connected in series in each said unit (S1-S6), and that the semiconductor elements belonging to the same unit are controlled by one and the same control pulse.

21. A method according to any of the preceding claims, **characterized** in that it is semiconductor elements (13-16) in the form of IGBTs (Insulated Gate Bipolar Transistors) that are controlled to be turned on and off.

22. A method according to any of the preceding claims, **characterized** in that it is carried out on a converter in the form of a VSC converter for conversion of ac voltage into dc voltage and vice versa, with said line formed from an ac-voltage phase conductor for generating, by changing between the main states, a train of pulses with definite amplitudes according to a pulse-width modulation pattern on the output (4) of the converter.

23. A method according to claim 22, **characterized** in that it is a VSC converter with a dc-voltage side formed from a dc-voltage network for transmission of high-voltage direct current (HVDC) and the ac-voltage phase conductor belonging to an ac-voltage network that is controlled.

24. A method according to claim 22, **characterized** in that it is two VSC converters of a back-to-back station with their ac-voltage sides connected to one and the same, or to separate, ac-voltage networks and their dc-voltage sides connected to each other that are controlled.

25. A method according to claim 22, **characterized** in that it is a VSC converter included in an SVC (Static Var Compensator) with the dc-voltage side formed from freely hanging capacitors and the ac-voltage phase conductor belonging to an ac-voltage network that is controlled.

26. A method according to any of claims 1-21, **characterized** in that it is a VSC converter with said output connected to an ac motor that is controlled.

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27. A method according to any of claims 1-21, **characterized** in that it is a VSC converter with said output connected to an ac generator that is controlled.

15 28. A converter for conversion of dc voltage into ac voltage or dc voltage and vice versa, comprising a series connection of four units (S1-S4), arranged between two poles, one positive pole (7) and one negative pole (8), of a first side in the form of a dc-voltage side of the converter, each of  
20 said units comprising a gate turn-off semiconductor element (13-16) and a diode (17-20) connected in antiparallel therewith and being given orders according to the order in the series connection from the positive to the negative pole, a line on the second side of the converter being connected to  
25 a first centre, designated output (4), of the series connection between the second and third units, means (9) arranged to provide, on said first side, a centre (23) between the two poles and to place these poles at the same voltage but with opposite signs in relation to the centre of the first  
30 side, wherein a second centre (24) of the series connection between the first and second units is connected, via a fifth said unit (S5) with a gate turn-off semiconductor element (10) and with the diode (26) connected in antiparallel therewith with the conducting direction with respect to the  
35 output (4) opposite to the conducting direction of the diode of the second unit, to the centre (23) of the first side, and a third centre (27) of the series connection between the third and fourth units is connected, via a sixth said unit (S6) with a gate turn-off semiconductor element (11) and

with the diode (29) connected in antiparallel therewith with a conducting direction with respect to the output opposite to the diode of the third unit, to the centre of the first side, wherein the converter also comprises a device (30) arranged to control the semiconductor elements of the units to be turned on and off to alternately achieve four main states of the converter in the form of a connection of the output to the positive pole (7) of the first side according to a first, to the negative pole (8) according to a second or to the centre (23) via any of two different so-called zero states, namely a third, in which the second and fifth units are in a conducting state, and a fourth, in which the third and sixth units are in a conducting state, wherein the first and sixth units form a pair in that the device is arranged to control the semiconductor elements thereof to assume, in the respective main state, the same position, turned on or off, and the fourth and fifth units form a pair in that the device is arranged to control the semiconductor elements thereof to assume, in the respective main state, the same position, turned on or off, and wherein the device is arranged to control the semiconductor elements such that a change between the first and second main states is always made via the third or fourth zero state, characterized in that the device is arranged, when changing between main states via a so-called small commutation loop, that is, changing between a connection of the positive pole to the output and the zero state according to the third main state, or a connection of the negative pole to the output and the zero state according to the fourth main state, at least when the current direction would entail a voltage peak on essentially the entire voltage between said positive pole (7) and said negative pole (8) across that of the second (S2) or the third (S3) unit which does not belong to the commutation loop in those cases where the semiconductor elements which are to be turned on in the coming main state and belong to a said pair of units were to be turned on simultaneously, to control these semiconductor elements according to an extra sequence in the form of a delayed turn-on of the semiconduc-



tor element in one unit of the latter pair relative to the semiconductor element in the other unit of said pair.

29. A computer program which is loadable directly into the  
5 internal memory of a computer, said computer program comprising software code portions for controlling the steps of any of claims 1-27, when running the program on the computer.

30. A computer program according to claim 29, provided at  
10 least partly via a network such as the Internet.

31. A computer-readable medium with a program registered  
thereon, wherein the program is designed to bring a computer  
to control the steps according to any of claims 1-27.

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